DATA SHEET

NE56625-20
System reset with Watchdog timer

Product data
Supersedes data of 2002 Mar 25

2003 Oct 15

Philips
Semiconductors

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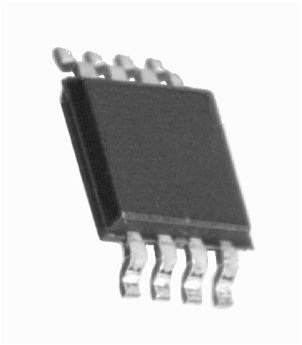
System reset with Watchdog timer NE56625-20

GENERAL DESCRIPTION

The NE56625-20 is comprised of a power-on reset, a Watchdog timer and low battery detection circuit. The NE56625 is designed to generate an Active-LOW reset signal for a variety of microprocessor and logic systems. Accurate reset signals are generated during momentary power interruptions or whenever power supply voltages sag to intolerable levels. The built-in Watchdog timer monitors the microprocessor and ensures it is operating properly. Any abnormal system operations due to microprocessor malfunctions are terminated by a system reset generated by the Watchdog. To accommodate a wide range of system requirements, the Watchdog Monitoring Time and power-on reset delay time are programmable from 10 ms to 10 sec.

The NE56625-20 is designed for low voltage battery powered applications with low battery detection threshold at 2.2 V. It is offered in the 8-lead small outline surface mount package (SOP005).



FEATURES

- Accurate threshold detection voltages:
  - Low battery: 2.2 V ±3%
  - Power-on reset: 2.0 V ±3%
- Low hysteresis voltage (both low battery check and power-on reset): 50 mV typ.
- Low supply current: 150 μA typ.
- Programmable power-on reset detection voltage
- Programmable power-on reset delay: 10 ms to 10 s
- Internal Watchdog timer programmable with external resistor and capacitor: 10 ms to 10 s
- Reset assertion with V_{CC} down to 0.8 V_{DC} (typical)
- Few external components required

APPLICATIONS

- Microcomputer systems and logic systems
- 2 V cordless phones
- Various portable, battery operated equipment

SIMPLIFIED SYSTEM DIAGRAM

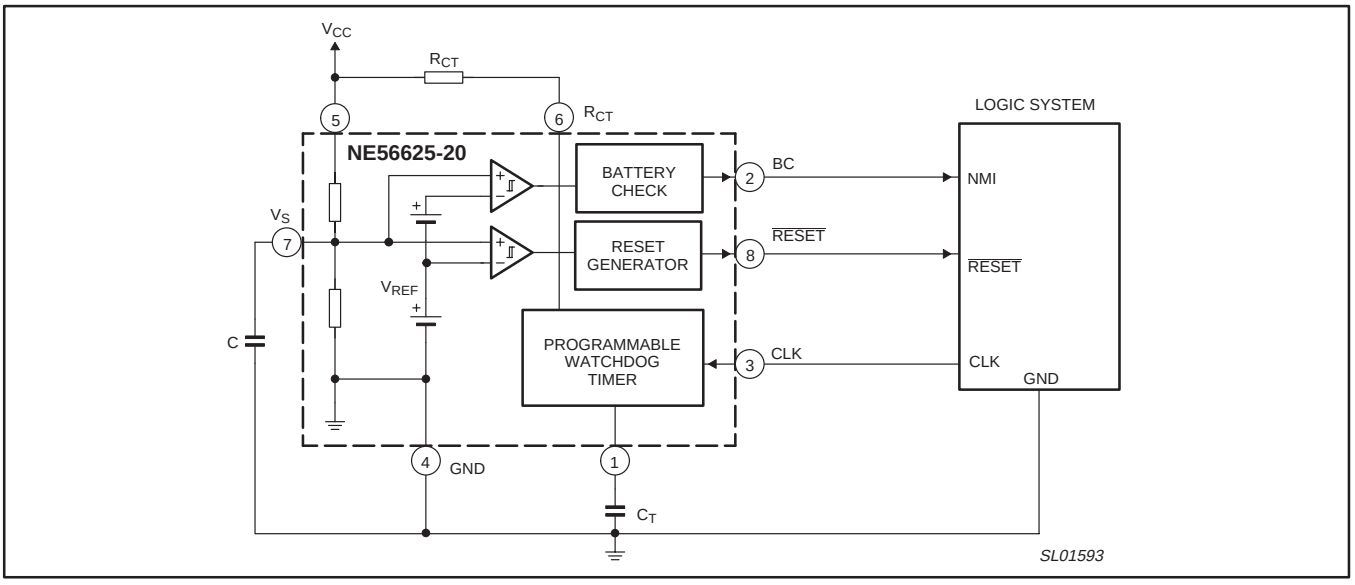


Figure 1. Simplified system diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE
	NAME	DESCRIPTION	VERSION	
NE56625-20D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOP005	–20 to +75 °C

PIN CONFIGURATION

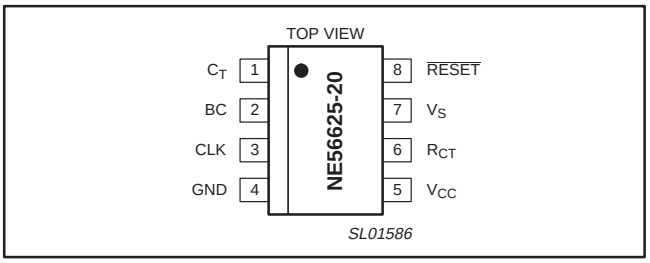


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	C_T	t_{WDM}, t_{WDR}, t_{PR} adjustment pin. t_{WDM}, t_{WDR}, t_{PR} times are dependent on the value of external C_T capacitor used. See Figure 17 (Timing Diagram) for definition of t_{WDM}, t_{WDR}, t_{PR} times.
2	BC	Battery check Active-LOW output.
3	CLK	Clock input pin from logic system for Watchdog timer.
4	GND	Circuit ground.
5	V_{CC}	Positive supply voltage.
6	R_{CT}	Watchdog timer control pin. The Watchdog timer is enabled when this pin is pulled-up to V_{CC} with a resistor, and disabled when this pin is connected to ground.
7	V_S	Detection threshold adjustment pin. The detection threshold can be decreased by connecting this pin to V_{CC} with a pull-up resistor. The detection threshold can be increased by connecting this pin to ground with a pull-down resistor.
8	$\overline{RESET}$	Reset Active-LOW output.

MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	Power supply voltage	–0.3	7	V
V_{VS}	V_S pin voltage	–0.3	7	V
V_{CLK}	CLK pin voltage	–0.3	7	V
V_{OH}	$\overline{RESET}$ and BC pin voltage	–0.3	7	V
T_{oper}	Operating temperature	–20	+75	°C
T_{stg}	Storage temperature	–40	+125	°C
P	Power dissipation	–	300	mW

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	1.9 to 6.5	V
I_{OLR}	$\overline{RESET}$ sink current	0 to 500	µA
I_{OLC}	BC sink current	0 to 5.0	mA
V_{CKH}	HIGH-level clock input voltage	< 1.0	V
V_{CKL}	LOW-level clock input voltage	< 0.2	V
t_{WD}	Clock monitoring time	1 to 10,000	ms
$t_{r(CLK)}$, $t_{f(CLK)}$	Clock rise and fall times	< 100	µs
$t_{r(VCC)}$	Power supply voltage rise time	< 100	µs
$t_{f(VCC)}$	Power supply voltage fall time	< 50	µs
T_{amb}	Operating ambient temperature	–20 to +70	°C
C_T	TC capacitance	0.0022 to 2.2	µF

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 2.6 V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CC}	Supply current during Watchdog timer operation	no load	–	0.7	1.0	mA
V_{SLR}	$\overline{RESET}$ detection threshold	V_{CC} = falling; R_{CT}: GND; V_S = open	1.94	2.0	2.06	V
$\Delta V_{SR}/\Delta T_{amb}$	Temperature coefficient of reset detection voltage	–20 °C ≤ T_{amb} ≤ 70 °C	–	±0.01	±0.05	%/°C
V_{hysR}	$\overline{RESET}$ threshold hysteresis	V_{CC} = falling; R_{CT}: GND; V_S = open	25	50	100	mV
V_{SLB}	Battery detection voltage	V_{CC} = falling; R_{LB} = 10 kΩ	2.13	2.20	2.27	V
$\Delta V_{SB}/\Delta T_{amb}$	Temperature coefficient of battery detection voltage		–	±0.01	±0.05	%/°C
V_{hysB}	Battery hysteresis voltage	V_{CC} = falling; R_{LB} = 10 kΩ	25	50	100	mV
ΔV_{SL}	Detection voltage difference	$\Delta V_{SL} = V_{SLB} - V_{SLR}$	175	200	225	mV
V_{TH}	CLK input threshold		0.8	1.2	2.0	V
I_{IH}	HIGH-level CLK input current	V_{CLK} = 2.6 V	–	0	1	µA
I_{IL}	LOW-level CLK input current	V_{CLK} = 0 V	–15	–6	–2	µA
V_{OHR}	HIGH-level output voltage, $\overline{RESET}$	$I_{\overline{RESET}}$ = –1.0 µA; V_S = open	2.0	2.2	–	V
V_{OHB}	HIGH-level output voltage, BC	R_{LB} = 10 kΩ	2.0	2.2	–	V
V_{OLR}	LOW-level output voltage, $\overline{RESET}$	$I_{\overline{RESET}}$ = 500 µA; V_{CC} = 1.8 V	–	0.3	0.5	V
V_{OLB}	LOW-level output voltage, BC	I_{BC} = 5 mA; V_{CC} = 1.8 V	–	0.3	0.5	V
I_{OLR}	$\overline{RESET}$ output sink current	$V_{\overline{RESET}}$ = 0.5 V; V_{CC} = 1.8 V	500	700	–	µA
I_{OLB}	Battery Check output sink current	V_{BC} = 0.5 V; V_{CC} = 1.8 V	5	7	–	mA
I_{OHR}	$\overline{RESET}$ output source current	$V_{\overline{RESET}}$ = 2.0 V	2	4	–	µA
I_{CT1}	C_T charge current	V_{CT} = 0.5 V; during Watchdog operation	–0.3	–0.15	–0.075	µA
I_{CT2}		V_{CT} = 0.5 V; during power-on reset operation	–0.3	–0.15	–0.075	µA
V_{CCL}	Supply voltage to assert reset operation	$V_{\overline{RESET}}$ = 0.4 V; $I_{\overline{RESET}}$ = 0.05 mA	–	0.8	1.0	V

AC ELECTRICAL CHARACTERISTICS

Characteristics measured with V_{CC} = 2.6 V, and T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{P1}	Minimum power supply pulse width for detection	4.0 V ≤ negative-going V_{CC} pulse ≤ 5.0 V	8.0	–	–	µs
t_{CLKW}	Clock input pulse width		3.0	–	–	µs
t_{CLK}	Clock input cycle		20	–	–	µs
t_{WDM}	Watchdog monitoring time (Notes 1, 6)	C_T = 0.022 µF; R_{CT} = open	50	100	150	ms
t_{WDR}	Watchdog reset time (Notes 2, 6)	C_T = 0.022 µF	1.0	2.0	3.0	ms
t_{PR}	Power-on reset delay time (Notes 3, 6)	V_{CC} = rising from 0 V; C_T = 0.022 µF	50	100	150	ms
t_{PDR}	$\overline{\text{RESET}}$ propagation delay time (Note 4)	V_{CC} = falling; R_{LR} = 100 kΩ; C_{LR} = 15 pF	–	10	–	µs
t_{PDB}	Battery Check propagation delay time (Note 4)	V_{CC} = falling; R_{LB} = 10 kΩ; C_{LB} = 15 pF	–	10	–	µs
t_{RR}	$\overline{\text{RESET}}$ rise time (Note 5)	R_{LR} = 100 kΩ; C_{LR} = 15 pF	–	10	–	µs
t_{FR}	$\overline{\text{RESET}}$ fall time (Note 5)	R_{LR} = 100 kΩ; C_{LR} = 15 pF	–	2	–	µs
t_{RB}	Battery Check rise time (Note 5)	R_{LB} = 10 kΩ; C_{LB} = 15 pF	–	10	–	µs
t_{FB}	Battery Check fall time (Note 5)	R_{LB} = 10 kΩ; C_{LB} = 15 pF	–	2	–	µs

NOTES:

1. 'Watchdog monitoring time' (t_{WDM}) is the duration from the last pulse (negative-going edge) of the timer clear clock pulse until reset output pulse occurs (see Figure 17). A reset signal is output if a clock pulse is not input during this time.
2. 'Watchdog reset time' (t_{WDR}) is the reset pulse width. Do not confuse this with the power-on reset delay time (t_{PR}).
3. The power-on reset delay or hold time is the duration measured from the time V_{CC} exceeds the upper detection threshold (V_{SHR}) and power-on reset release is experienced ($\overline{\text{RESET}}$ output HIGH).
4. 'Reset response time' is the duration from when the supply voltage sags below the lower detection threshold (V_{SL}) and reset occurs ($\overline{\text{RESET}}$ output LOW).
5. Reset rise and fall times and Battery Check rise and fall times are measured at 10% and 90% output levels.
6. Watchdog monitoring time (t_{WDM}), Watchdog reset time (t_{WDR}), and power-on reset delay time (t_{PR}) during power-on can be modified by varying the C_T capacitance. The times can be approximated by applying the following formula. The recommended range for C_T is 0.0022 µF to 2.2 µF.

Formula 1. Calculation for approximate t_{PR}, t_{WDM}, and t_{WDR} values:

t_{PR} (ms) ≈ 4500 × C_T (µF)
t_{WDM} (ms) ≈ 4500 × C_T (µF)
t_{WDR} (ms) ≈ 90 × C_T (µF)

Example: When C_T = 0.022 µF and R_{CT} = open:

t_{PR} ≈ 100 ms
t_{WDM} ≈ 100 ms
t_{WDR} ≈ 2.0 ms

TYPICAL PERFORMANCE CURVES

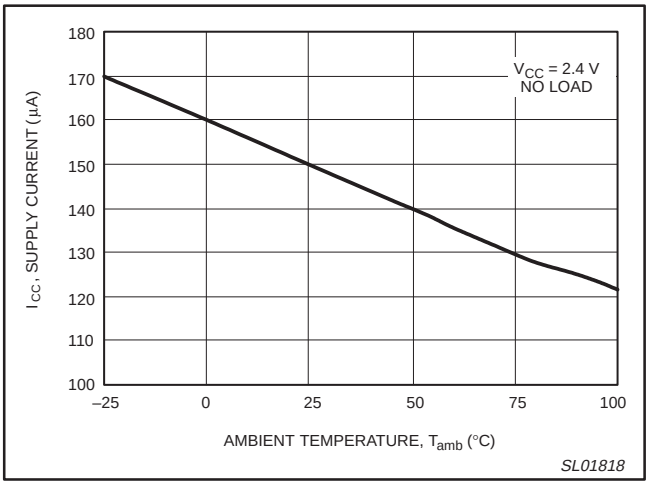


Figure 3. Supply current versus ambient temperature.

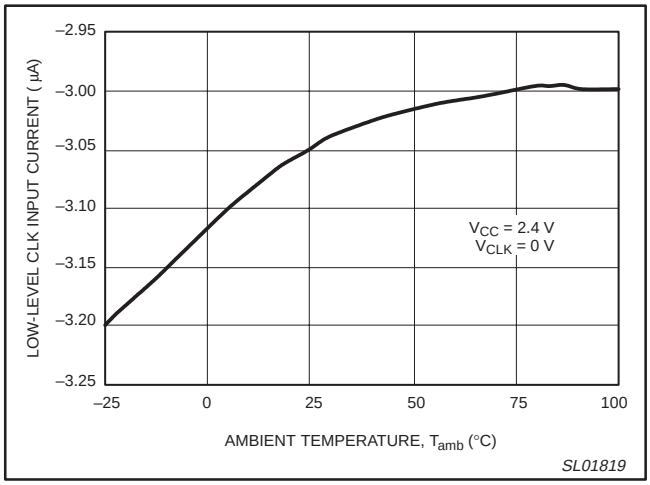


Figure 4. LOW-level CLK input current versus ambient temperature.

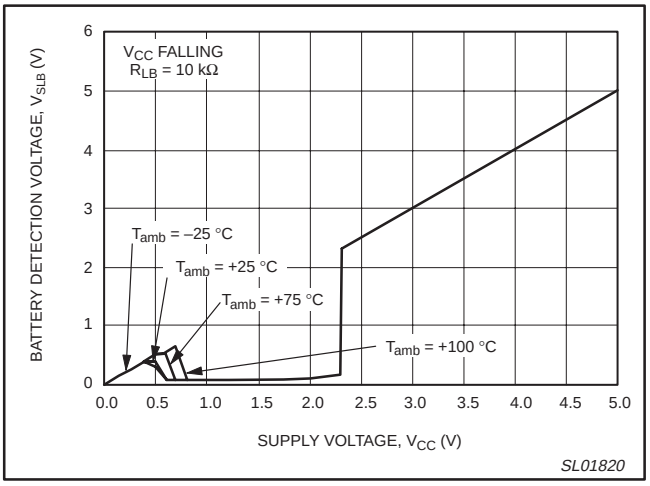


Figure 5. Battery detection votlage versus supply voltage.

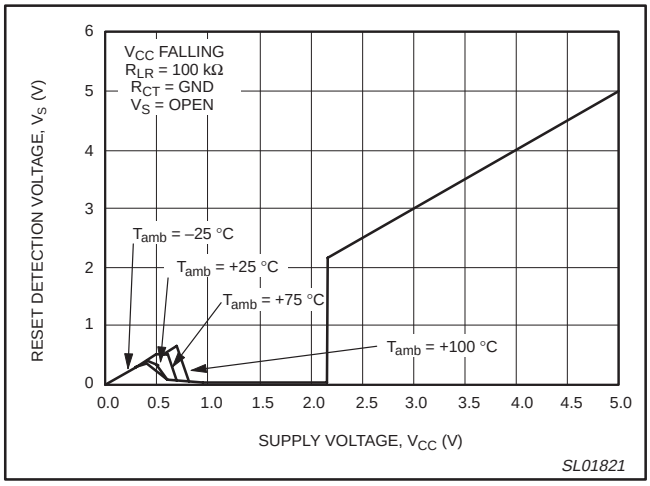


Figure 6. RESET detection voltage versus supply voltage.

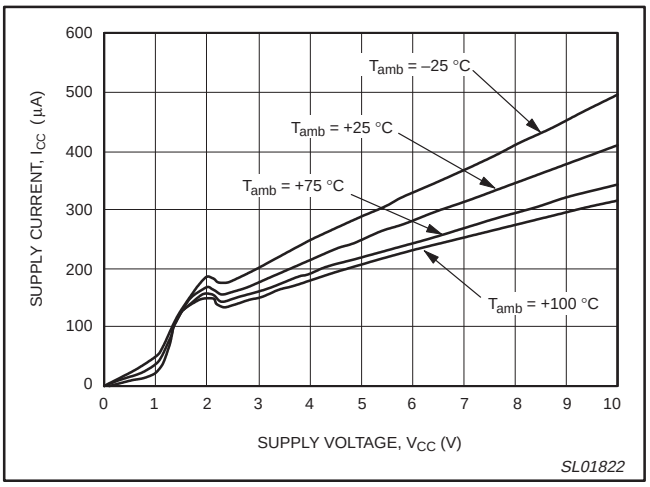


Figure 7. Supply current versus supply voltage.

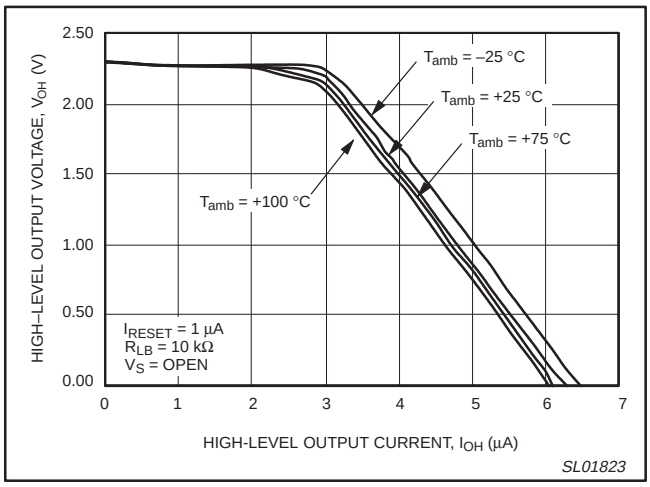


Figure 8. HIGH-level output voltage versus HIGH-level output current

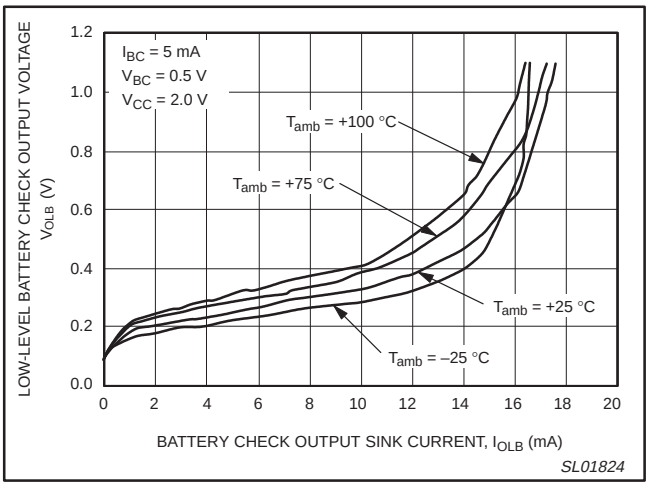


Figure 9. Battery check LOW-level output voltage versus battery check output sink current

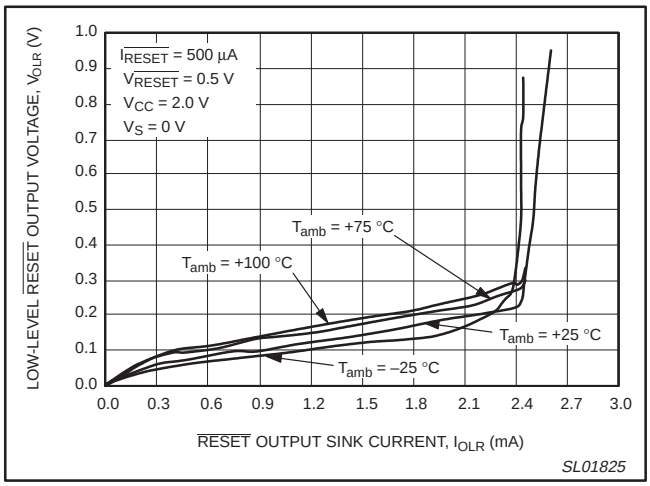


Figure 10. LOW-level $\overline{\text{RESET}}$ output voltage versus $\overline{\text{RESET}}$ output sink current.

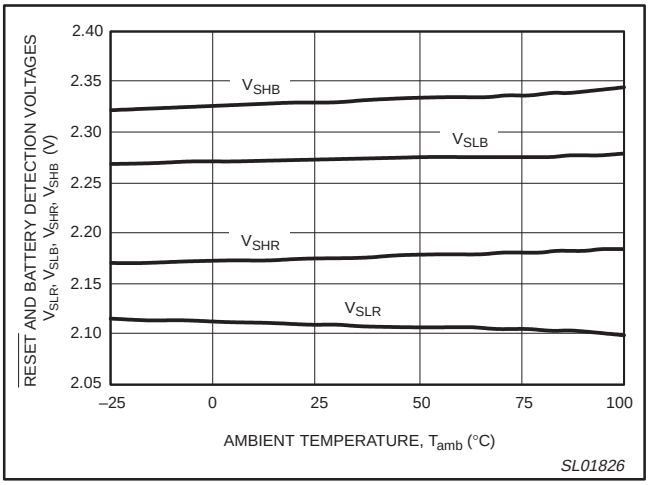


Figure 11. $\overline{\text{RESET}}$ and battery detection voltages versus temperature.

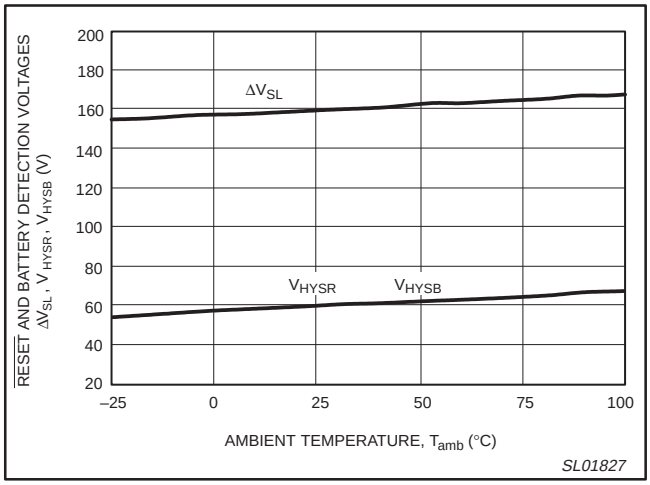


Figure 12. $\overline{\text{RESET}}$ and battery hysteresis voltages versus temperature.

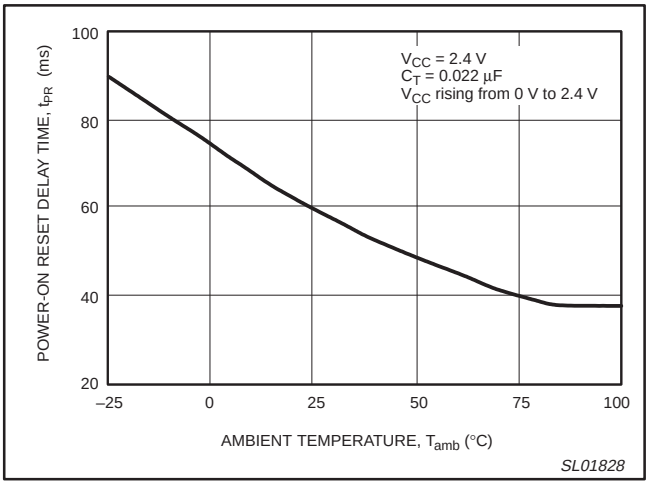


Figure 13. Power-on reset delay time versus temperature.

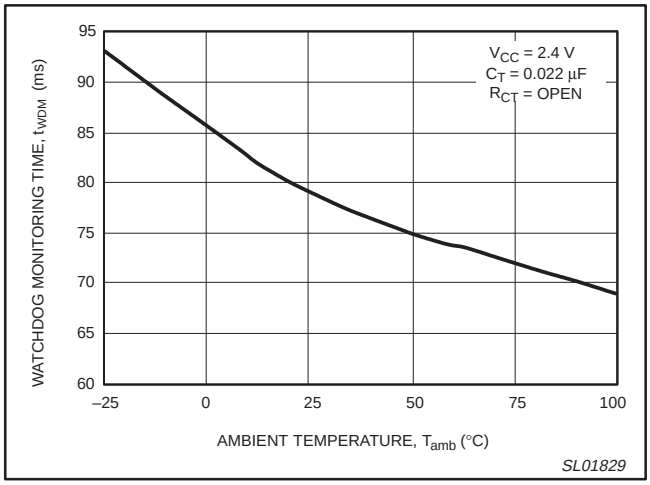


Figure 14. Watchdog monitoring time versus temperature.

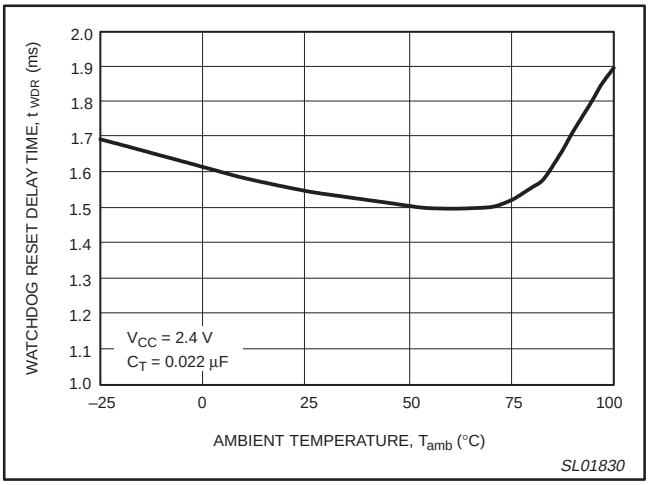


Figure 15. Watchdog reset delay time versus temperature.

TECHNICAL DESCRIPTION

The NE56625-20 combines a Watchdog timer, a Battery Check and an Undervoltage Reset functions in a single SO8 surface mount package. This provides a space-saving solution for maintaining proper operation of typical 2.0 volt cordless telephone and other low voltage portable, handheld communication and industrial equipment.

While the Watchdog monitors the microprocessor operation, the Battery Check and Undervoltage Reset monitor the supply voltage to the microprocessor. If the microprocessor clock signal ceases or becomes erratic, the NE56625-20 outputs a reset signal to the microprocessor. If the microprocessor supply voltage sags to 2.0 volts or less, the NE56625-20 outputs a reset signal for the duration of the supply voltage deficiency. The Undervoltage Reset signal allows the microprocessor to shut down in an orderly manner to avoid system corruption. In addition to a $\overline{\text{RESET}}$ output, the NE56625-20 has a Battery Check output for system use. If the supply voltage sags below 2.2 volts or less, the Battery Check output goes LOW and remains LOW until the supply voltage recovers. Both the undervoltage detection threshold and battery check detection threshold incorporate hysteresis to prevent generating erratic resets.

The Watchdog timer requires a pulse input. Normally this signal comes from the system microprocessor's clock. For operation, pin 6 is not connected (open) or an external resistor (R_{CT}) of 1 MΩ or greater is connected from Pin 6 to V_{CC} and an external capacitor (C_T) is placed from Pin 1 to ground. The recommended range for C_T capacitor is 2.2 nF to 2.2 µF. The external R_{CT} resistor and C_T capacitor establish the required minimum frequency of Watchdog input signal for the device to **not** output a reset signal. The R_{CT} resistor establishes, in part, the rate of charge of the C_T capacitor. In the absence of a Watchdog input pulse, the C_T capacitor charges to the 0.2 volt threshold of the internal comparator, causing a reset signal to be output. If microprocessor clock signals are received within the required interval, no Watchdog reset signal will be output. The Watchdog function can be disabled by grounding Pin 6 without affecting the undervoltage detection function.

Although the temperature coefficient of detection threshold is specified over a temperature of –20 °C to +70 °C, the device will support operation in excess of this temperature range. See the supporting curves for performance over the full temperature range of –25 °C to +100 °C. Some degradation in performance will be experienced at the temperature extremes and the system designer should take this into account.

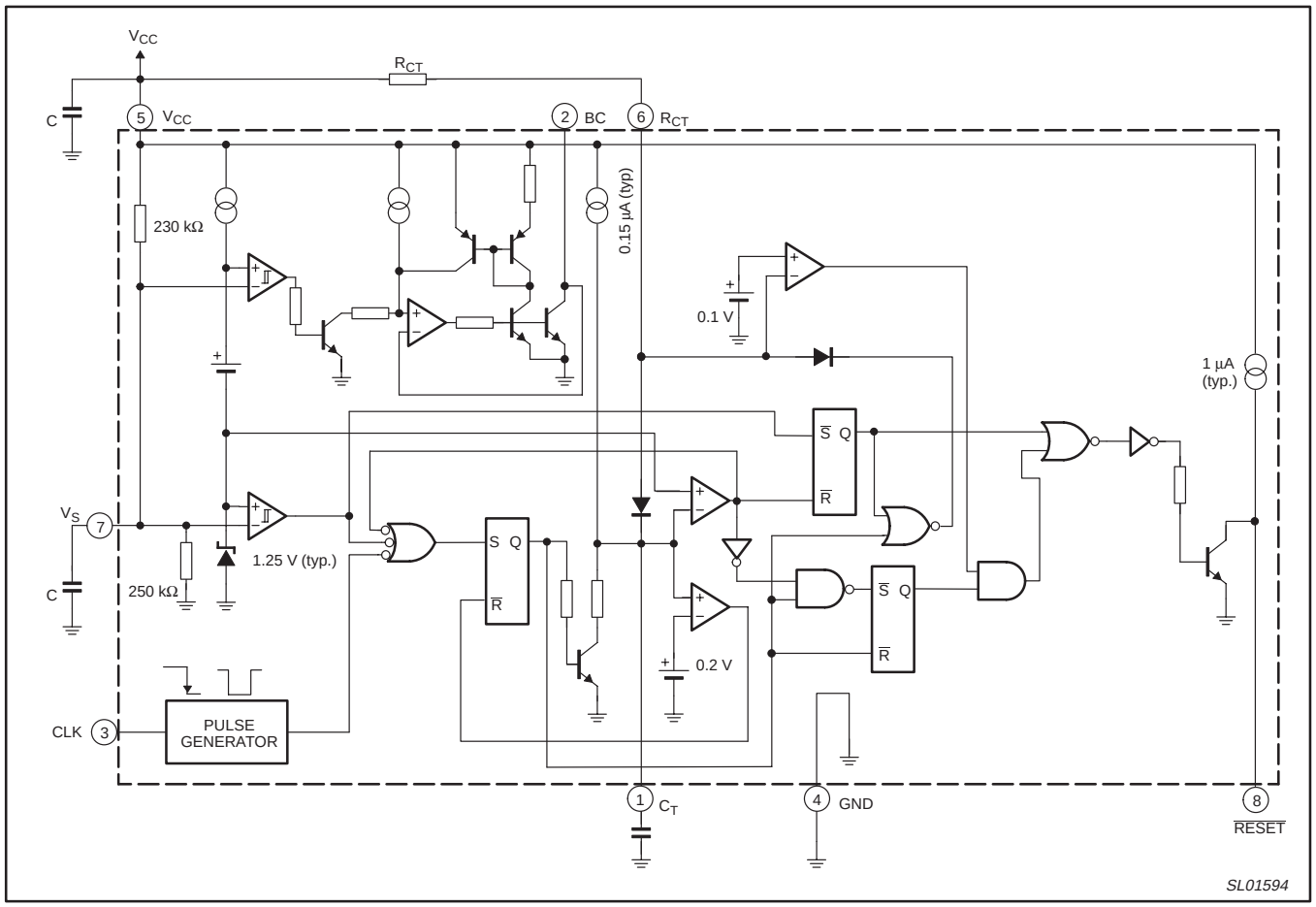


Figure 16. Functional diagram.

Timing diagram

The timing diagram shown in Figure 17 depicts the operation of the device. Letters indicate events on the TIME axis.

A: At start-up 'A', the V_{CC} voltage begins to rise. Also the $\overline{\text{RESET}}$ and Battery Check (BC) voltages initially rise, but then abruptly return to a LOW state. This is due to V_{CC} reaching the level of 0.8 V that activates the internal bias circuitry, asserting $\overline{\text{RESET}}$ and BC.

B: Just before 'B', the C_T voltage starts to ramp up. This is caused by, and coincident to, V_{CC} reaching the threshold level of V_{SHR}. At this level the device initiates the $\overline{\text{RESET}}$ delay time, t_{PLH}. V_{CC} continues to rise above V_{SHR}.

C: At 'C', V_{CC} rises to the threshold level of V_{SHB}, the upper voltage BC detection threshold. At this level, the BC output goes HIGH. BC output follows V_{CC} to its normal operating level.

D: At 'D', V_{CC} is above the undervoltage detect threshold and C_T has ramped up to its upper detect level. At this point, an internal ramp discharge transistor activates, discharging C_T. Reset assertion is still in effect since the delay time has not elapsed.

E: At 'E', the delay time has elapsed and the device removes the hold on the reset. $\overline{\text{RESET}}$ goes HIGH.

In a microprocessor based system these events remove the reset from the microprocessor, allowing it to function normally. The system must send clock signals to the Watchdog Timer often enough to prevent C_T from ramping up to the C_T threshold, to prevent reset signals from being generated. Each clock signal discharges C_T.

E–F: Midway between 'E' and 'F', the CLK signals cease allowing the C_T voltage to ramp up to its $\overline{\text{RESET}}$ threshold at 'F'. At this time reset signals are generated ($\overline{\text{RESET}}$ goes LOW). The device attempts to come out of reset as the C_T voltage is discharged, and finally does come out of reset when CLK signals are reestablished after two attempts of C_T.

G–I: Immediately before 'G', falling V_{CC} causes the $\overline{\text{RESET}}$ and BC outputs to sag. CLK signals are still being received, and C_T is within normal operating range. V_{CC} continues to sag until the V_{SLB} battery check undervoltage threshold is reached. At that time (G), BC output goes LOW. V_{CC} sags still further until V_{SLR} reset undervoltage threshold is reached. At this point (H), reset is asserted and $\overline{\text{RESET}}$ goes LOW. Between 'H' and 'I', V_{CC} starts to rise, however, C_T voltage does not start to ramp up until 'I', when V_{CC} reaches the V_{SHR} upper reset threshold. Also, the RESET delay is initiated.

J–K: At 'J', the BC output goes HIGH when V_{CC} rises to V_{SHB}. Between 'J' and 'K, C_T reaches the upper threshold level again. At 'K', $\overline{\text{RESET}}$ delay time elapses and the reset is released and $\overline{\text{RESET}}$ goes HIGH.

L–M: From 'L' to 'M', the R_{CT} is shorted to ground. This disables the Watchdog timer by shorting C_T to ground. At other times R_{CT} is open or taken to V_{CC} with a resistor of 1 MΩ or greater. This configuration enables the Watchdog timer.

N: After 'N', normal CLK signals are received, but at a lower frequency than those following event 'D'. The frequency is above the minimum frequency required to keep the device from outputting reset signals.

O–P: At 'O', V_{CC} is normal, CLK signals are being received, and no reset signals are output. At event 'P', the V_{CC} starts falling, causing $\overline{\text{RESET}}$ and BC to also fall.

Q: At event 'Q' V_{CC} sags to the point where the V_{SLR} undervoltage threshold point is reached, and at that level reset signal is outputted ($\overline{\text{RESET}}$ to a LOW state).

R: At event 'R' the V_{CC} voltage has deteriorated to a level where normal internal circuit bias is no longer able to maintain a $\overline{\text{RESET}}$, and as a result may exhibit a slight rise to something less than 0.8 V. As V_{CC} decays even further, $\overline{\text{RESET}}$ also decreases to zero.

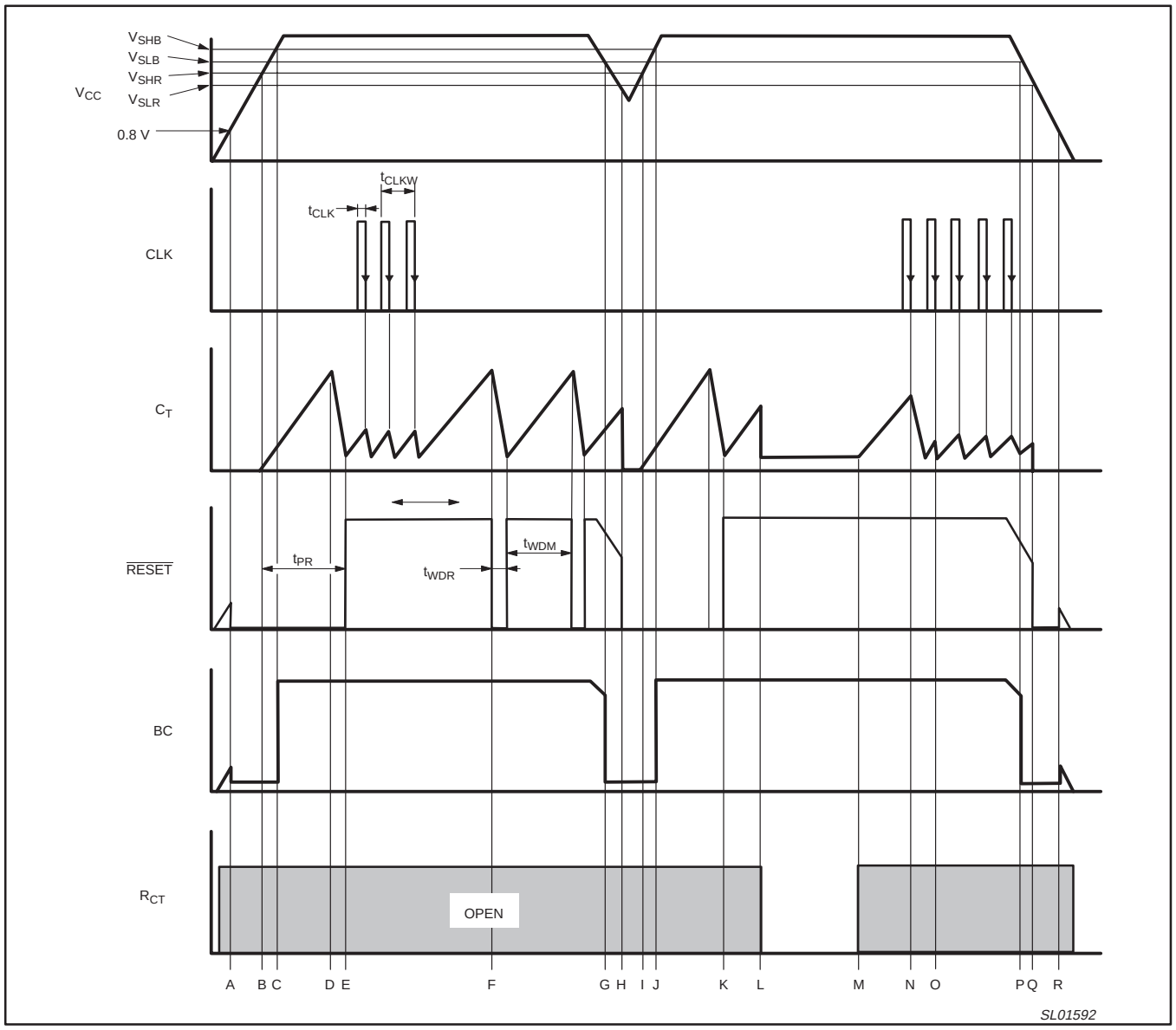


Figure 17. Timing diagram.

APPLICATION INFORMATION

Detection threshold

The detection threshold voltage can be adjusted by externally influencing the internal divider reference voltage. Figures 18 and 20 show a method to raise and lower the threshold voltage. Figures 19 and 21 show the influence of the pull-down and pull-up resistors on the threshold voltage. The use of a capacitor (1000 pF or larger) from pin 7 to ground is recommended to filter out noise from being imposed on the threshold voltages.

The Reset Detection Threshold can be increased by connecting an external resistor R_1 from Pin 7 to ground, as shown in Figure 18. See Figure 19 to determine the approximate value of R_1 to use. The threshold made be varied somewhat linearly from 2.4 V to 3.0 V.

The Reset Detection Threshold can be decreased by connecting an external resistor R_2 from Pin 7 to V_{CC}, as shown in Figure 20. See Figure 21 to determine the approximate value of R_2 to use. The lower thresholds may be varied in a linear fashion from 1.85 V to 1.65 V.

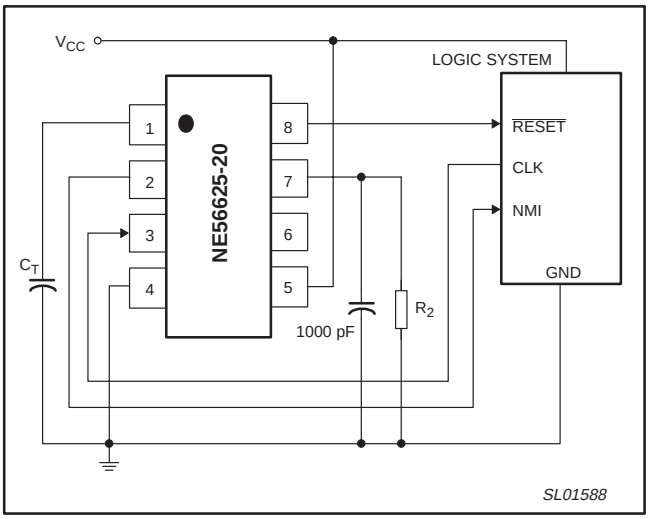


Figure 18. Circuit to raise detection threshold.

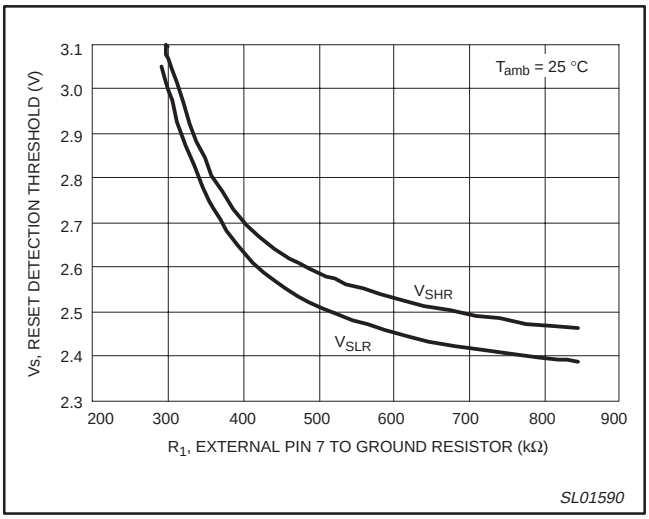


Figure 19. Reset detection threshold versus external R_1.

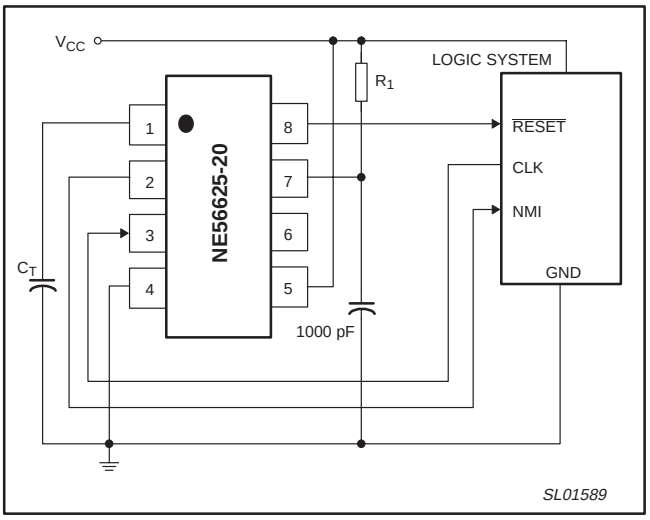


Figure 20. Circuit to lower detection threshold.

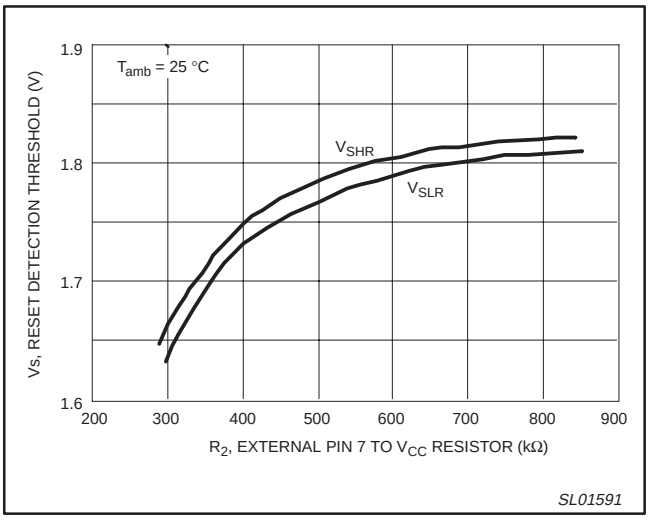


Figure 21. Reset detection threshold versus external R_2.

Watchdog monitoring time

The Watchdog timer's external component values are critical to its performance.

The values of R_{CT} and C_T affect the Watchdog monitoring time (t_{WDM}), the Watchdog reset time (t_{WDR}), and power-on reset delay time (t_{PR}). See Formula 1 in the AC Electrical Characteristics and the timing diagram shown in Figure 17 for parameter definitions.

The effect of RCT on the Watch-Dog Timer Monitoring Time at room temperature for CT = 0.0022 µF is shown in Figure 22.

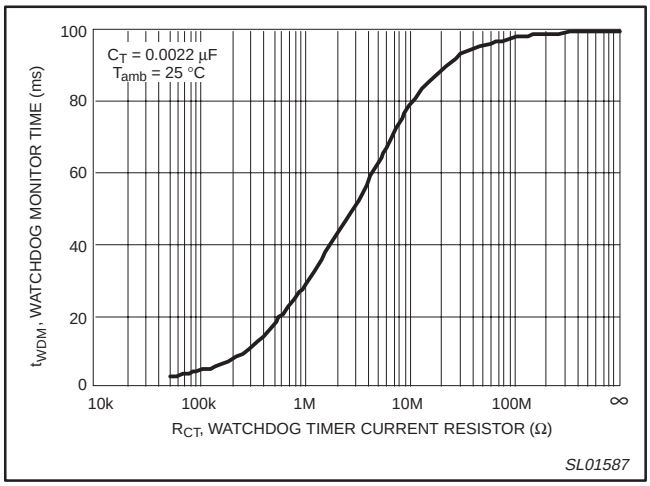


Figure 22. Watchdog monitoring vs. pull-up resistor R_{CT}.

PACKING METHOD

The NE56625-20 is packed in reels, as shown in Figure 23.

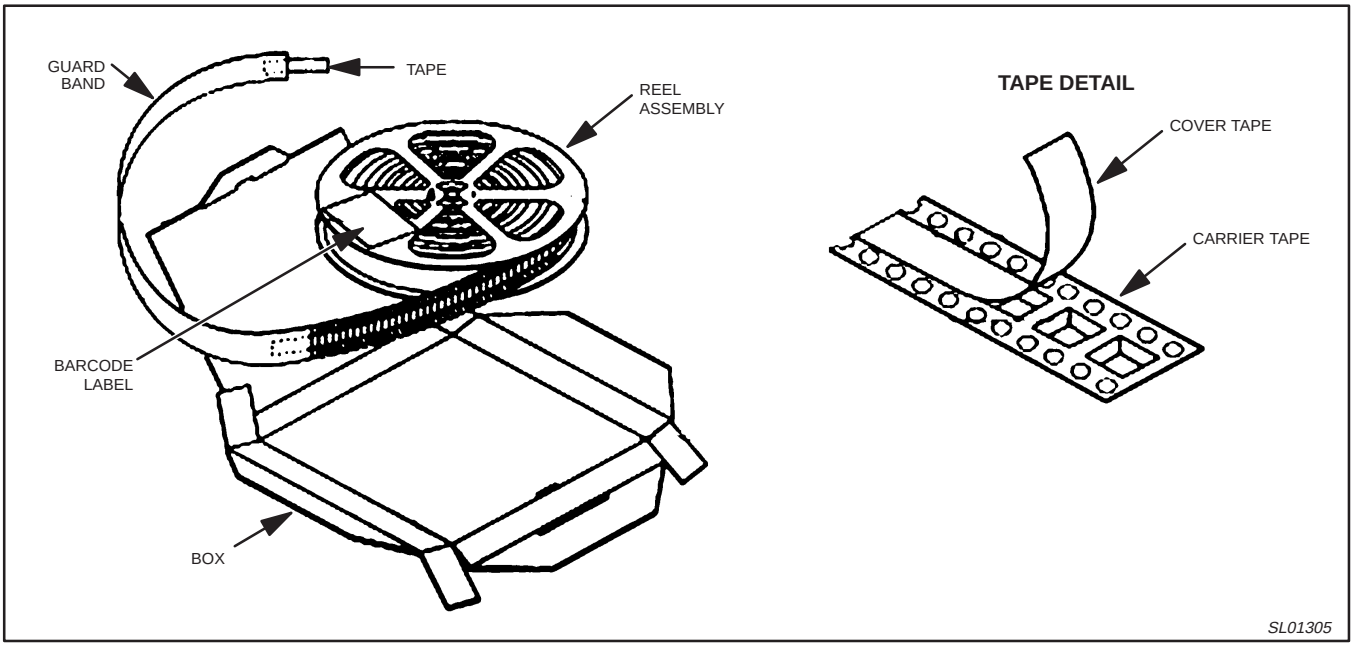
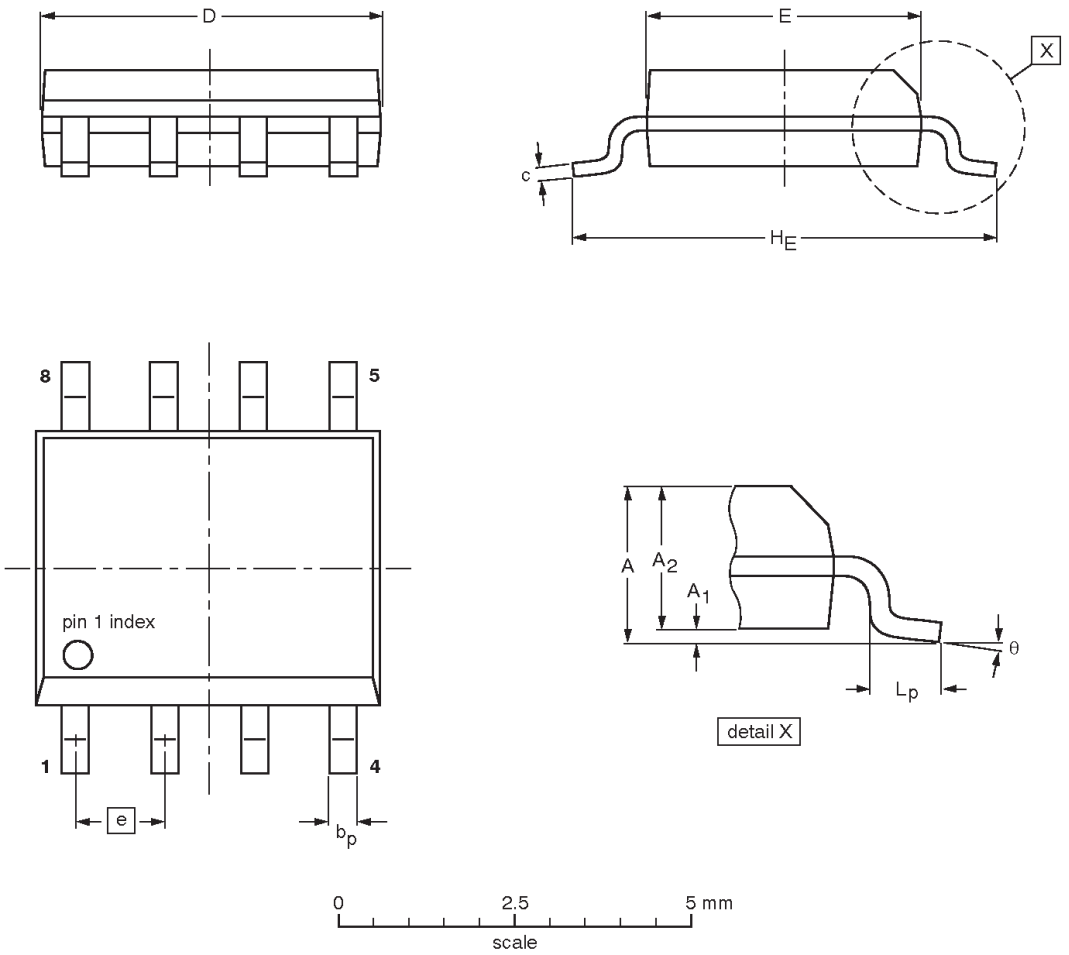


Figure 23. Tape and reel packing method.

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOP005**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	b_p	c	D(1)	E(2)	e	H_E	L_p	θ
mm	1.73	0.25 0.10	1.45 1.25	0.51 0.33	0.25 0.19	4.95 4.80	4.0 3.8	1.27	6.2 5.8	1.27 0.38	8° 0°
inches	0.068	0.010 0.004	0.057 0.049	0.013 0.020	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.050 0.015	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOP005	076E03	MS-012				03-10-07

REVISION HISTORY

Rev	Date	Description
_2	20031015	**Product data (9397 750 12124). ECN 853-2327 30314 of 08 September 2003. Supersedes data of 2002 Mar 25 (9397 750 09645).** Modifications: ● Change package version to SOP005 in Ordering information and Package outline sections.
_1	20020325	**Product data (9397 750 09645). ECN 853-2327 27919 of 25 March 2002.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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